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Description

ANALOG-TO-DIGITAL CONVERTER UTILIZING A TIMER FOR INCREASED RESOLUTION

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an analog-to-digital converter, and more specifically, to an analog-to-digital converter that calculates a digital output voltage based on a time required to charge a capacitor.

[0003] 2. Description of the Prior Art

[0004] Conventionally, analog-to-digital converters are used to convert an analog input voltage into a digital output voltage of a fixed resolution, which determines the precision of the analog-to-digital converter. Each analog-to-digital converter is usually rated to handle a specific range of analog input voltages to avoid saturating the analog-to-digital converter.

[0005] Please refer to Fig.1. Fig.1 is a schematic diagram of an analog-to-digital converter 10 according to the prior art. The analog-to-digital converter 10 contains input pins 16 and 18 for inputting an analog voltage to the analog-to-digital converter 10. Input pins 12, 14, and 20 are respectively used for providing a voltage input, a ground reference, and a voltage reference to the analog-to-digital converter 10. The analog-to-digital converter 10 calculates an analog voltage difference across input pins 16 and 18, converts the analog voltage into a digital output voltage, and outputs the digital output voltage on a plurality of output pins 25. The number of output pins 25 depends on the resolution of the analog-to-digital converter 10, and the analog-to-digital converter 10 shown in Fig.1 has n output pins 25 corresponding to an n-bit resolution. For example, an eight-bit resolution would require eight output pins 25 to output the digital output voltage.

[0006] Unfortunately, the analog-to-digital converter 10 contains a fixed resolution which is determined according to the complexity of the circuitry inside the analog-to-digital converter 10. Changing the resolution of the analog-to-digital converter 10 requires designing the analog-

to-digital converter 10 all over from scratch, and very little of the original design can be salvaged.

SUMMARY OF INVENTION

[0007] It is therefore a primary objective of the claimed invention to provide an analog-to-digital converter utilizing a timer for conveniently adjusting the resolution of the analog-to-digital converter in order to solve the above-mentioned problems.

[0008] According to the claimed invention, an analog-to-digital converter includes at least one input pin for receiving an analog input voltage, a capacitor for storing charge and producing a voltage across the capacitor, and a current source for flowing current through the capacitor for charging the capacitor. The analog-to-digital converter also contains a first switch electrically connected between the current source and the capacitor for controlling flow of current from the current source to the capacitor, a comparator for outputting a first comparison value when the analog input voltage is approximately equal to the voltage across the capacitor, and a timer for calculating a charging period of time needed for the voltage across the capacitor to become equal to the analog input voltage. Before the capacitor is charged, it is discharged to remove

all remaining charge. Then, the timer starts calculating the charging period of time when the first switch electrically connects the current source to the capacitor for charging the capacitor and stops calculating the charging period of time when the comparator outputs the first comparison value. A controller is used for controlling operation of the first switch, for starting the timer when the first switch electrically connects the current source to the capacitor for charging the capacitor, for stopping the timer when the comparator outputs the first comparison value, and for converting the charging period of time calculated by the timer into a digital output voltage.

[0009] It is an advantage of the claimed invention that resolution of the analog-to-digital converter can easily be adjusted by changing the clock rate of the timer. The analog-to-digital converter can be used in a variety of applications that require a range of different resolutions, or for any application that requires high resolution and for which a fast conversion time is not critical.

[0010] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various

figures and drawings.

Brief Description of Drawings

[0011] Fig.1 is a schematic diagram of an analog-to-digital converter according to the prior art.

[0012] Fig.2 is a block diagram of an analog-to-digital converter according to the present invention.

[0013] Fig.3 is a graph showing input voltage values versus the corresponding charging times calculated by the timer.

[0014] Fig.4 is a flowchart illustrating converting the analog input voltage to a digital output voltage according to the present invention method.

Detailed Description

[0015] Please refer to Fig.2. Fig.2 is a block diagram of an analog-to-digital converter 50 according to the present invention. The analog-to-digital converter 50 contains a capacitor C which is used to store charge and produce a voltage Vc across the capacitor C. The capacitor C is electrically connected to a constant current source 58 through a first switch 56. When the first switch 56 is turned on, current Ic flows from the constant current source 58 through the capacitor C for charging the capacitor C and raising the voltage Vc across the capacitor C. When the

first switch 56 is turned off, the current Ic cannot flow through the capacitor C. Since the current Ic produced by the constant current source 58 is constant, the voltage Vc increases linearly with respect to time during the interval in which the current Ic flows through the capacitor C.

[0016] An analog input voltage Vin is input across two input pins P1 and P2, although it is also possible to use a single input pin if the input voltage Vin shares a common ground with the analog-to-digital converter 50. A comparator 52 compares the input voltage Vin with the voltage Vc and produces an output signal EQL. When the input voltage Vin is approximately equal to the voltage Vc, the output signal EQL is equal to "1". Otherwise, the value of the output signal EQL is equal to "0".

[0017] A second switch 54 is electrically connected between the capacitor C and ground. Before flowing current Ic through the capacitor C, the second switch 54 should be turned on to discharge the capacitor C. Once the capacitor C is fully discharged, the second switch 54 is then turned off again. A controller 60 is used to control operation of the analog-to-digital converter 50. The controller 60 uses I/O1 and I/O2 pins to respectively control the first and second switches 56 and 54.

[0018] The controller 60 contains a timer 62 for calculating a charging time needed to charge the capacitor C. When the controller 60 turns on the first switch 56 to flow current Ic through the capacitor C, the controller 60 simultaneously turns on the timer 62 to start calculating the charging time. The controller 60 then monitors the value of the output signal EQL with an I/O3 pin to determine when the voltage Vc is equal to the input voltage Vin. When the output signal EQL is equal to "1", the controller 60 stops the timer 62 and reads the charging time calculated by the timer 62. At the same time, the first switch 56 is turned off to stop charging the capacitor C. The controller 60 then converts the charging time into a digital output voltage. The resolution of the analog-to-digital converter 50 is mainly dependent on the characteristics of the timer 62. The higher the resolution of the timer 62 is, the higher the resolution of the analog-to-digital converter 50 can be. Moreover, the clock rate of the timer 62 can be adjusted to change the resolution of the analog-to-digital converter 50. In order for the controller 60 to convert the charging time into the digital output voltage, the controller 60 will have to be calibrated according to the values of the current Ic outputted from the constant current

source 58, the characteristics of the capacitor C, and the characteristics of the timer 62.

[0019] Please refer to Fig.3. Fig.3 is a graph showing input voltage Vin values versus the corresponding charging times calculated by the timer 62. The fact that the voltage Vc increases linearly with the amount of time that the current Ic flows through the capacitor C enables the timer 62 to provide accurate calculation of the input voltage Vin. As Fig.3 shows, the higher the input voltage Vin is, the longer the charging time will be until the voltage Vc becomes equal to the input voltage Vin.

[0020] Please refer to Fig.4. Fig.4 is a flowchart illustrating converting the analog input voltage Vin to a digital output voltage according to the present invention method. Steps contained in the flowchart will be explained below.

[0021] Step 100:Start;

[0022] Step 102:Provide an analog input voltage Vin to the two input pins P1 and P2;

[0023] Step 104:Begin discharging the capacitor C by turning on the second switch 54; during this time, the first switch 56 should be turned off so as to not allow the current Ic to flow through the capacitor C;

[0024] Step 106:After the capacitor C has been fully discharged

so that voltage Vc is equal to zero, turn off the second switch 54; the first switch 56 is still turned off during this time;

[0025] Step 108:Reset the timer 62 to have a value of "0";

[0026] Step 110:Turn on the first switch 56 to begin charging the capacitor C, and simultaneously start the timer 62 to begin calculating the charging time;

[0027] Step 112:When the voltage Vc across the capacitor C is equal to the input voltage Vin, the comparator 52 generates the output signal EQL having a value equal to "1". The controller 60 reads the value of the output signal EQL, and stops the timer 62, and the first switch 56 is simultaneously turned off to stop charging the capacitor C;

[0028] Step 114:The controller 60 converts the charging time calculated by the timer 62 into a digital output voltage, thereby converting the analog input voltage Vin to the digital output voltage; and

[0029] Step 116:End.

[0030] In order for the present invention analog-to-digital converter 50 to work well, the accuracy of the charging timer 62 calculated by the timer 62 is critical. The controller 60 can easily direct the starting time of the timer 62 since the

controller 60 starts the timer at the same time as when the first switch 56 is turned on. To stop the timer 62, the controller 60 needs to have a means to monitor the value of the output signal EQL. To monitor the status of the output signal EQL, the controller 60 can periodically poll the value of the output signal EQL. Alternatively, the output signal EQL changing from a value of "0" to a value of "1" can generate an interrupt in the controller 60, thereby informing the controller 60 that it should stop the timer 62.

[0031] In contrast to the prior art, the resolution of the present invention analog-to-digital converter 50 can easily be adjusted by changing the characteristics of the timer 62. A clock rate of the timer 62 can be raised to provide an instant increase in the resolution of the analog-to-digital converter 50.

[0032] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.